ECE3056 - Architecture, Concurrency, and Energy in Computation (3-0-3)

Prerequisites: ECE 2031/20X2 [min C] and ECE 2035/3035 [min C]
Corequisites: None

Catalog Description: Basic organizational principles of the major components of computer processors: cores, memory hierarchy, and the I/O subsystem. Implications for performance, concurrency, and energy.

Textbook(s):
Patterson & Hennessey, *Computer Organization and Design: The Hardware/Software Interface* (5th edition), Morgan Kaufmann, 2014. ISBN 0124077269 (required)

Topical Outline:

1. Instruction Set Architectures
   a. Instructions, addressing modes, and sample ISAs
   b. Multi-cycle data path and control
   c. Controller implementation: state machine vs. microprogramming

2. Pipelining
   a. Pipelining basics
   b. Pipeline stages: fetch, decode, execute, memory write-back
   c. Hazards and solutions
   d. Branch prediction and delayed branches
   e. Case Studies

3. Memory Systems
   a. Basic organization of caches and main memory
   b. Virtual memory basics, memory management

4. Concurrency
   a. Evolution to multicore
   b. Introduction to synchronization primitives and the concept of data coherence
   c. Basics of message passing communication

5. Parallelism
   a. ILP, DLP, TLP
   b. Basic architectural support mechanisms

6. I/O Architectures
   a. Buses and interconnects
   b. Interrupts, DMA, polling
   c. Disk structures, I/O scheduling
   d. LANs, network interfaces, & basic interprocessor communication
   e. Case Studies

7. Energy and Power dissipation
   a. Dynamic and static energy dissipation fundamentals

b. Microarchitecture-level energy dissipation and power models
c. Power virus, kernel benchmarks and power
d. Basics of voltage and frequency scaling
e. Case studies

8. Project Assignments

Project assignments will use prepackaged architecture simulators and hardware description languages (HDLs). Three categories of assignments are conducted: i) datapath, ii) memory hierarchy, iii) power/energy